



MS-7388 VER:0A

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD RD780/RX780

ATI SB600

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111B/RTL8111C

HD Codec --ALC888&883

BIOS -- SPI ROM 8M

1394 -- VT6308

ESATA-SIL3531

Main Memory:

DDR II X 4 (Max 8GB)

Expansion Slots:

PCI-E X 1 *2(RX780)

PCI-E X 16 *1(RX780)

PCI-E X 1 *1(FOR RD780)

PCI-E X 16 *2(FOR RD780)

PCI 2.2 Slot X 2

PWM:

Controller--Intersil ISL6323 4 Phase

Vcore 3 Phase (MOS HIGHX2 LOWX2)

Vnb 1 Phase (MOS HIGHX1 LOWX2)

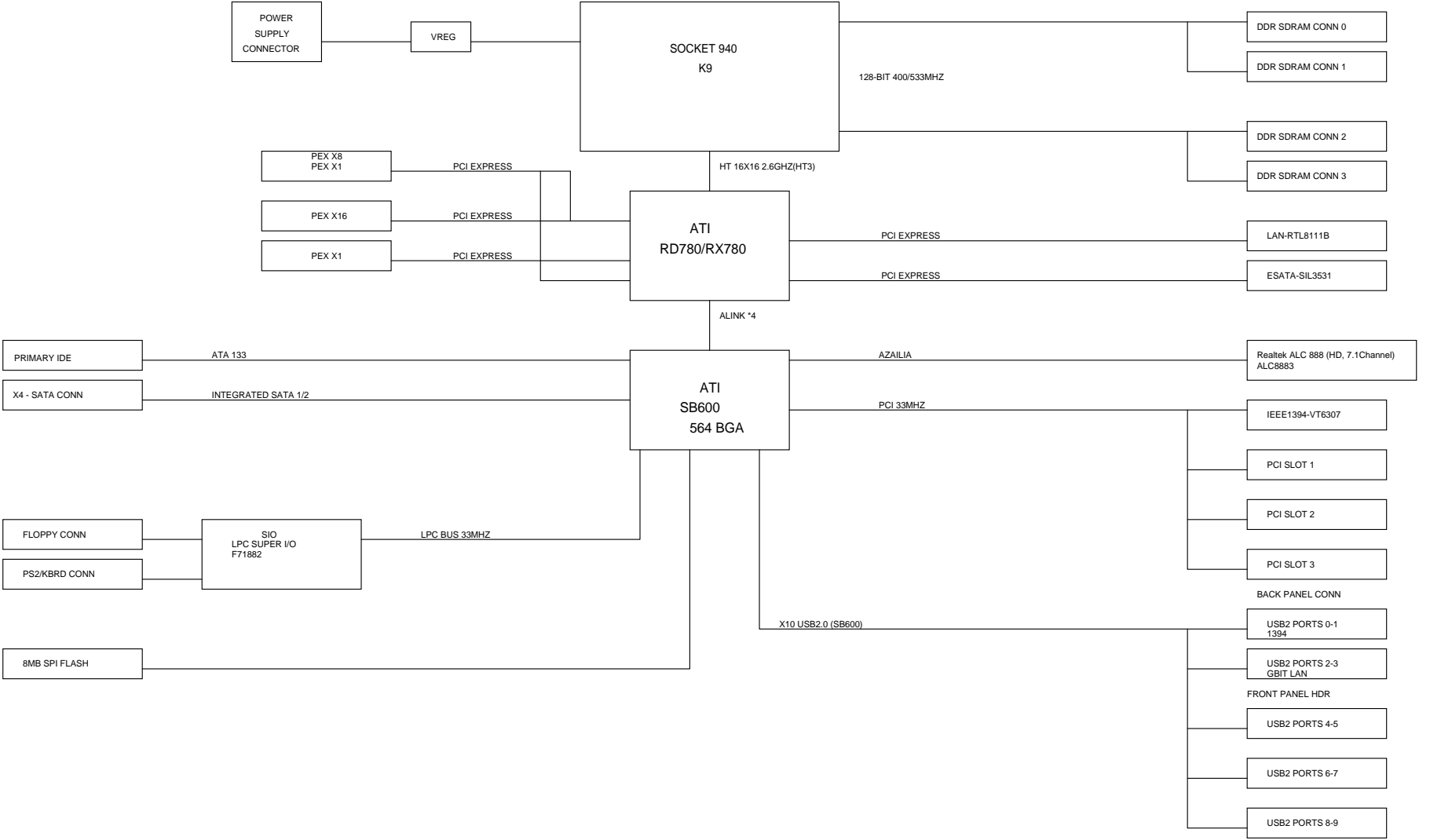
Clock Generator:

Controller--ICS9LPRS472

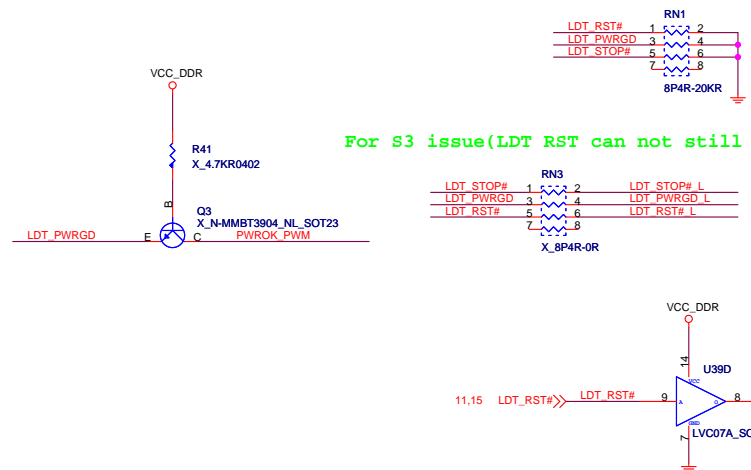
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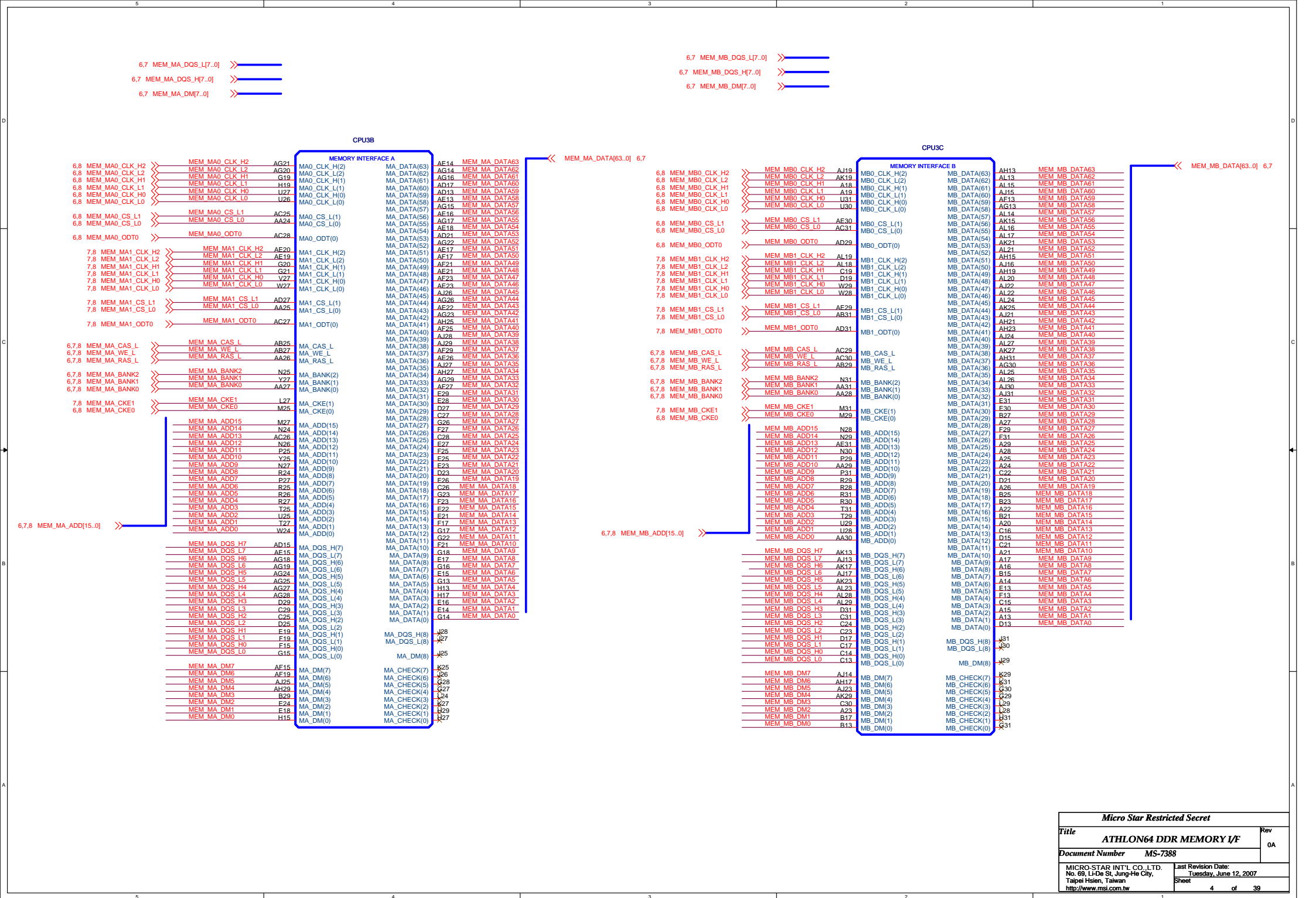
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222222
X_manual part

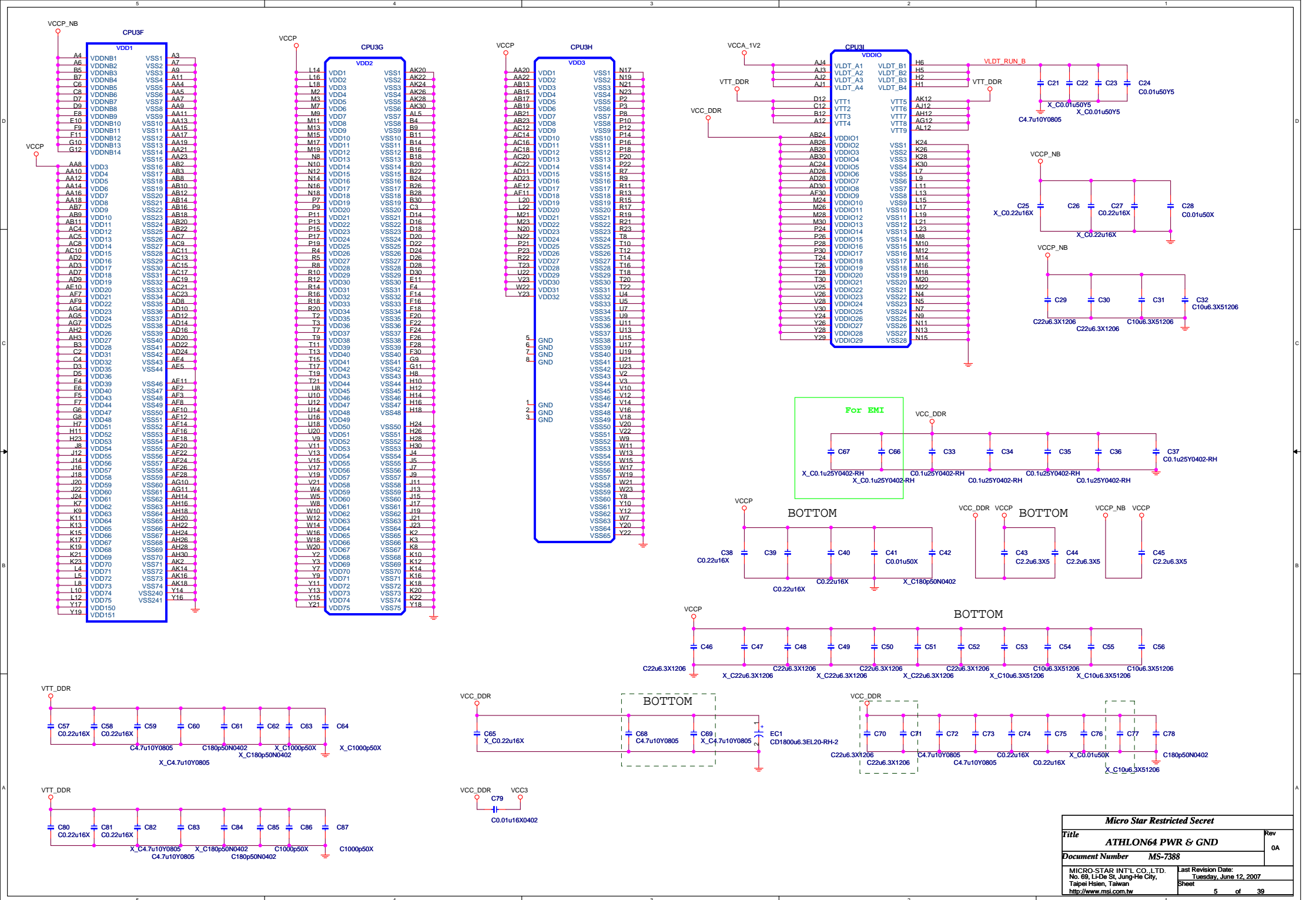
BLOCK DIAGRAM

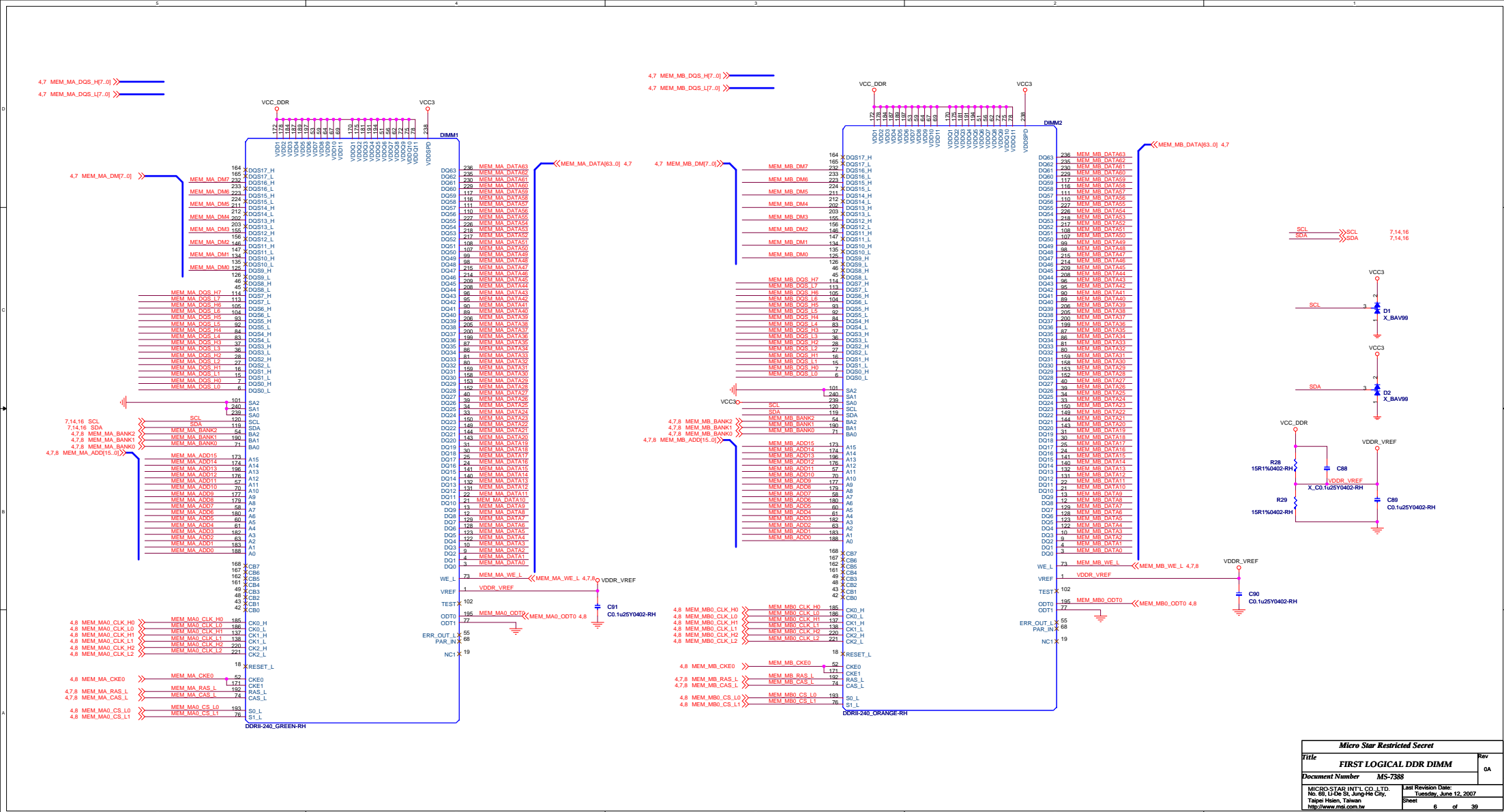


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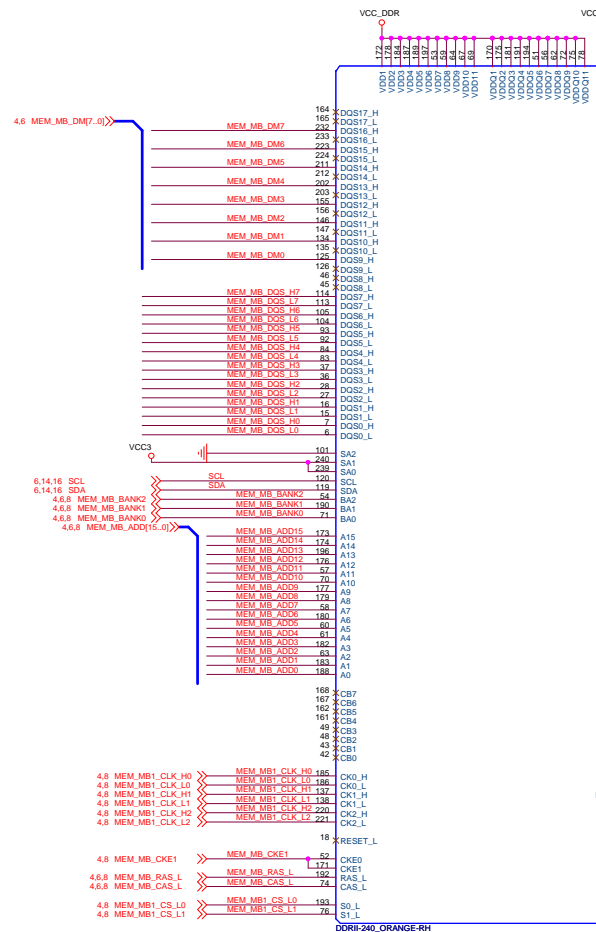




4.6 MEM_MA_DQS_H[7..0] >> >>
4.6 MEM_MA_DQS_L[7..0] >> >>



4.6 MEM_MB_DQS_L[7..0] >> >>
4.6 MEM_MB_DQS_H[7..0] >> >>



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Rev 0A

SECOND LOGICAL DDR DIMM

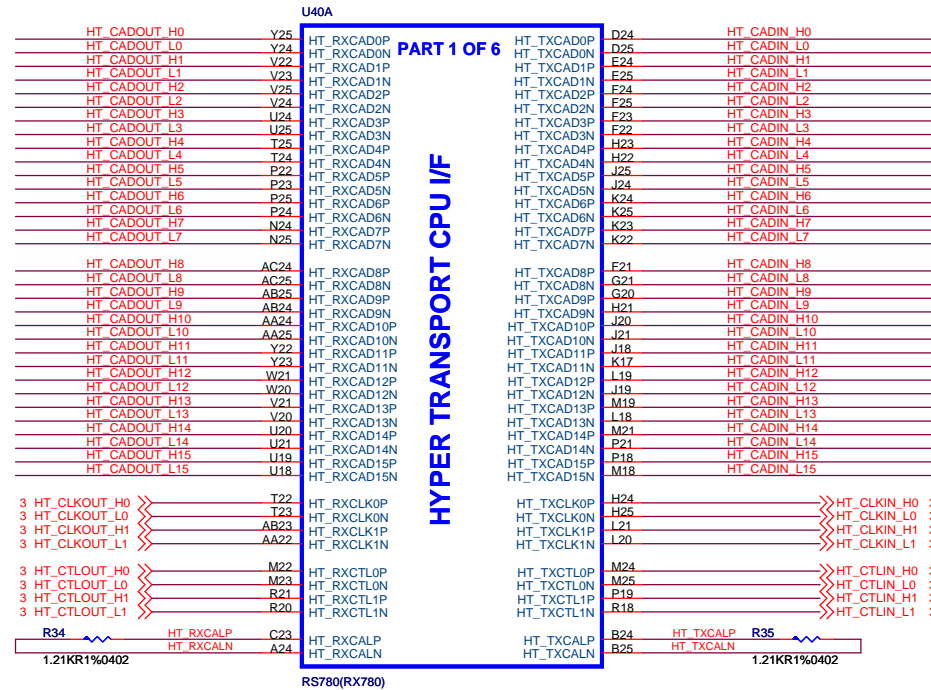
Document Number MS-7388

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3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780/RS780
HT_RXCALP	49.9R (GND)	1.21K
HT_RXCALN	49.9R (VDDHT)	
HT_TXCALP	100R	1.21K
HT_TXCALN		

REF

RD780

X_RD780

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```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT_GPI01
RX780: pin DFT_GPI01
RS780: pin SUS_STAT#
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
   thru nbcfg register)
0 : Enable
RX780: pin DFT_GPI00
RS780: configurable thru register
      setting only
RS740: Not supported
```

CRT/TVOUT

PM	PLL PWR
LVTM	

CLOCKS

MIS.

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	RED(GFNT_DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLDN	LVDS_BLDN
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPND	TMDS_HPND
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

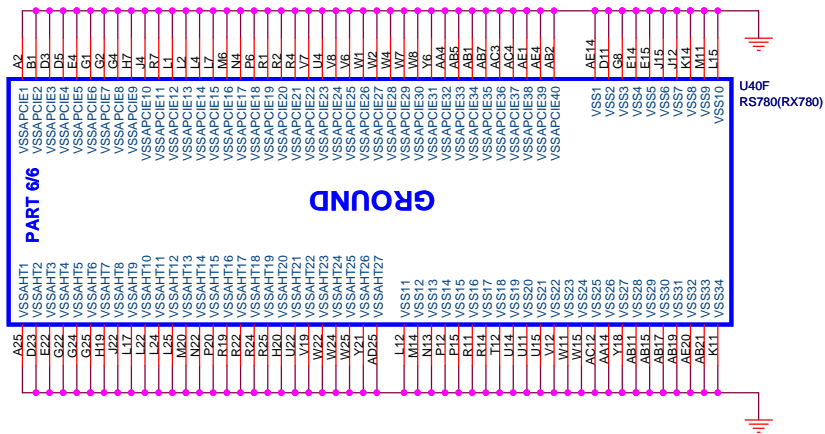
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U40D		
PAR 4 OF 6		
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)
AA12	MEM_A4(NC)	MEM_DQ4(NC)
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)
AC14	MEM_A12(NC)	MEM_DQ12(NC)
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)
AD16	MEM_BA0(NC)	MEM_DQ14/DVO_D10(NC)
AE17	MEM_BA1(NC)	MEM_DQ15/DVO_D11(NC)
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)
		MEM_DQS0N/DVO_IDCKN(NC)
W12	MEM_RASb(NC)	MEM_DQS1P(NC)
Y12	MEM_CASb(NC)	MEM_DQS1N(NC)
AD18	MEM_WEB(NC)	
AB13	MEM_CSb(NC)	MEM_DM0(NC)
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)
Y14	MEM_ODT(NC)	
V15	MEM_CKP(NC)	IOPLLVD18(NC)
W14	MEM_CKN(NC)	IOPLLVD(NC)
AE12	MEM_COMPP(NC)	IOPLLVS(NC)
AD12	MEM_COMPN(NC)	MEM_VREF(NC)
RS780(RX780)		

Note: If the Side-port memory interface is **not** used, make sure that:

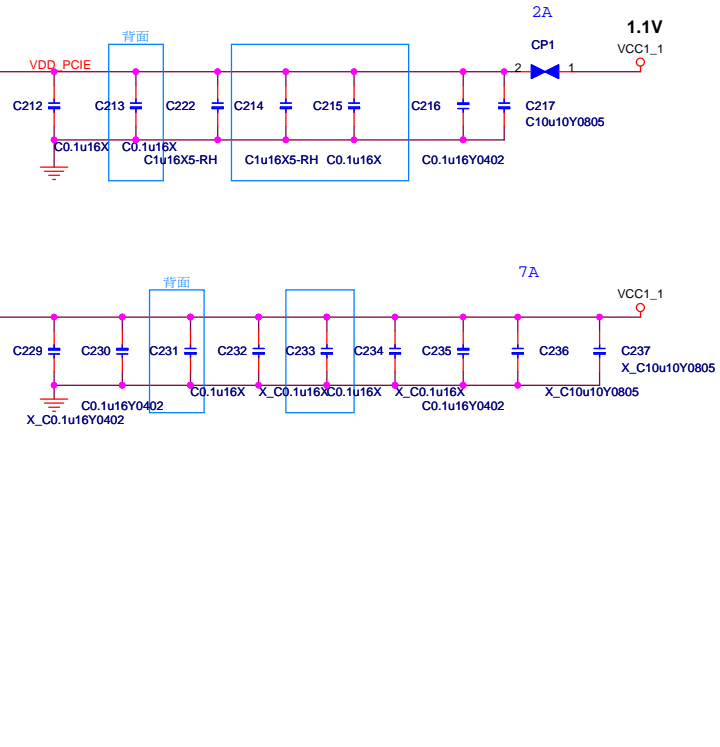
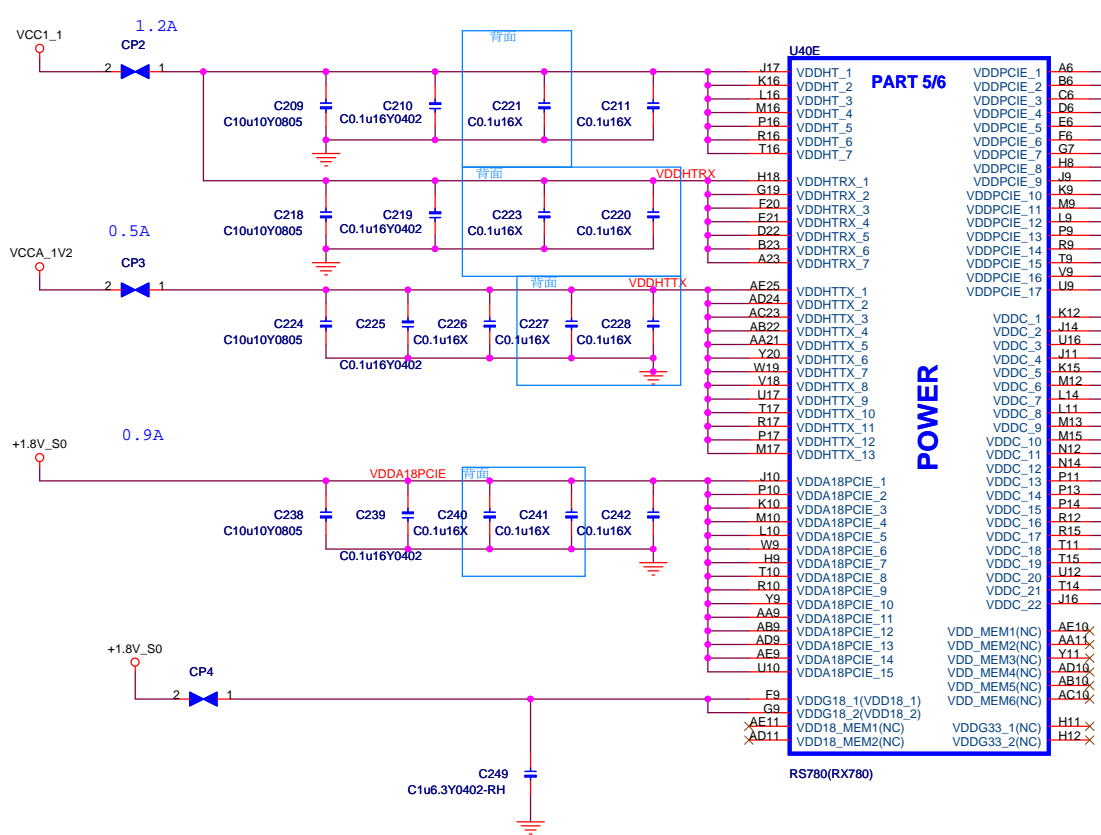
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

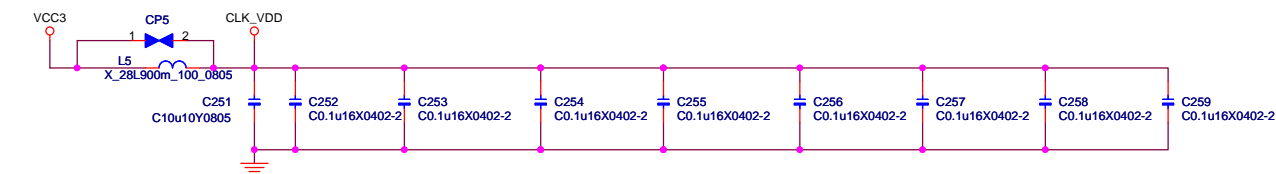
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Document Number MS-7388		
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC





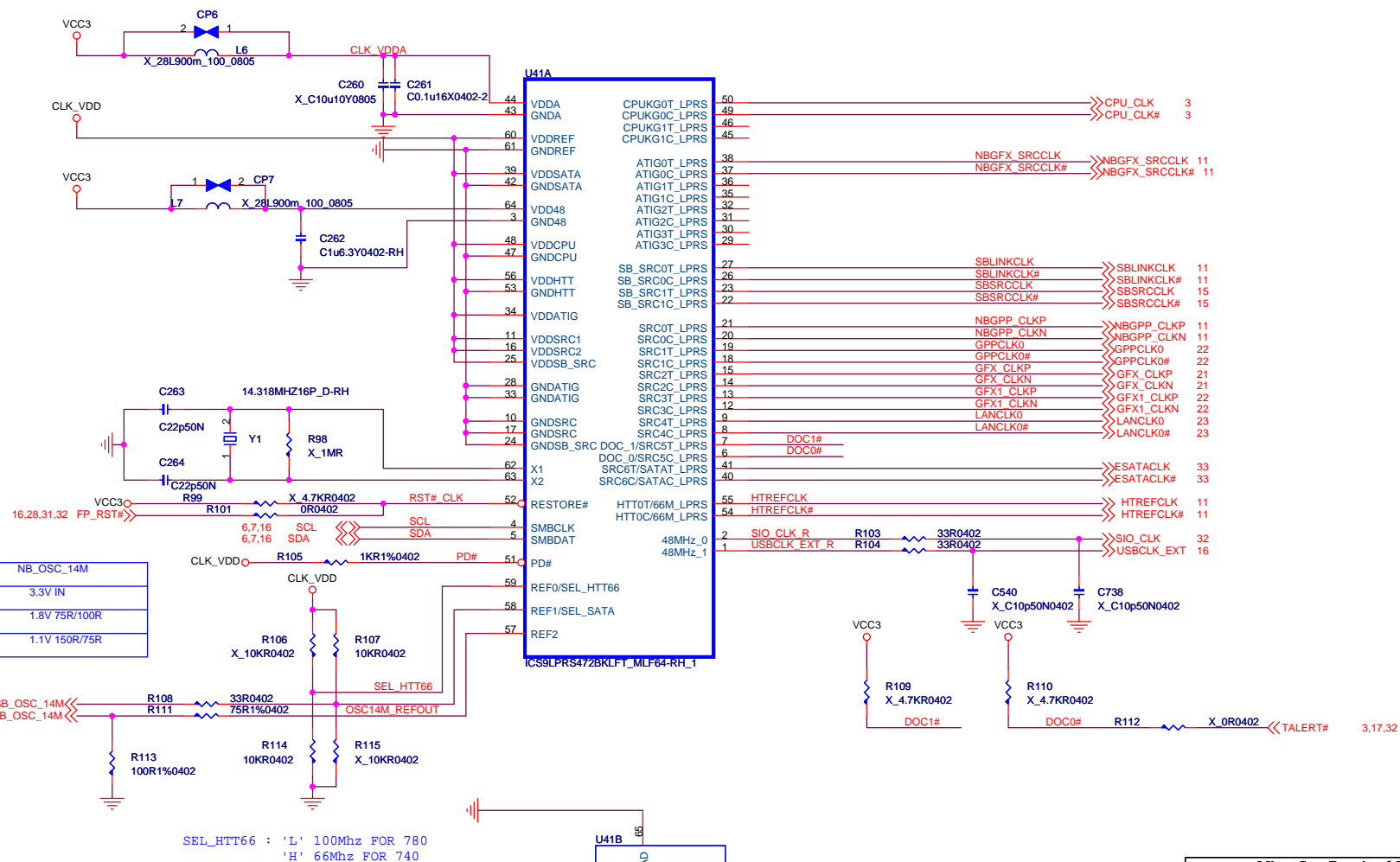
- ```

1- PLACE ALL THE SERIES TERMINATION
RESISTORS AS CLOSE AS U41 AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE

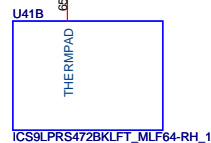
3- PUT DECOUPLING CAPS CLOSE TO U41
POWER PIN

```



|       |               |
|-------|---------------|
|       | NB_OSC_14M    |
| RS740 | 3.3V IN       |
| RX780 | 1.8V 75R/100R |
| RS780 | 1.1V 150R/75R |

```
SEL_HTT66 : 'L' 100Mhz FOR 780
 'H' 66Mhz FOR 740
```



FOR SB600 VCC\_SB= 1.2V

PLACE THESE COMPONENTS CLOSE TO U600, AND  
USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2

FOR SB460, THIS BALL(AH26) IS LDRQ1 ONLY  
FOR SB460, THIS BALL(W22) IS BMREQ# ONLY

Normal --> 1-2  
Clear CMOS --> 2-3

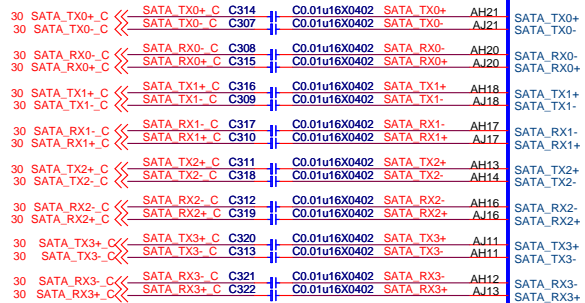
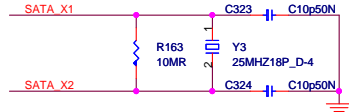
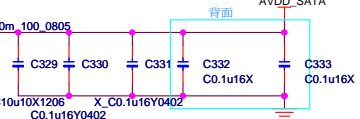
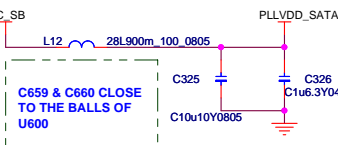
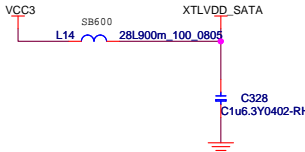
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| Document Number                                                                                               | MS-7388               |                                                                    |
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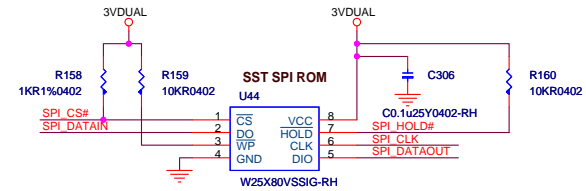
FOR SB600

PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600PLACE R665 CLOSE  
TO U600 BALL  
R674 IS 1K 1% FOR XTAL,  
4.99K 1% FOR INTERNAL CLKC658 CLOSE TO THE  
BALL OF U600SB600 SB 23x23mm  
Part 2 of 4

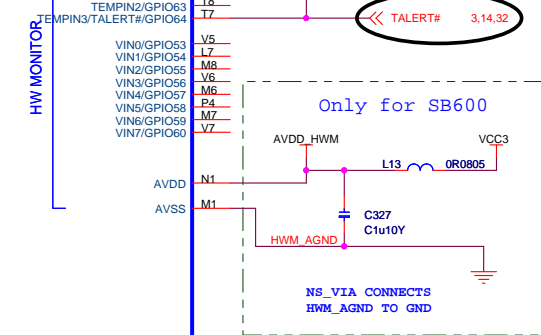
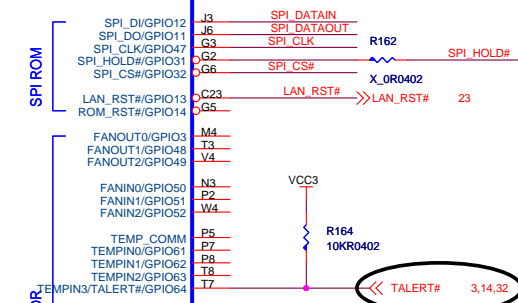
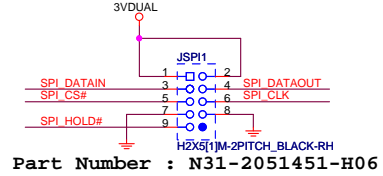
SERIAL ATA

SERIAL ATA POWER

AT1-SB600-218S6ECLA13FG-A13-RH



SPI FLASH MEMORY

SPI DEBUG PORT  
Place close to SPI ROM

Micro Star Restricted Secret

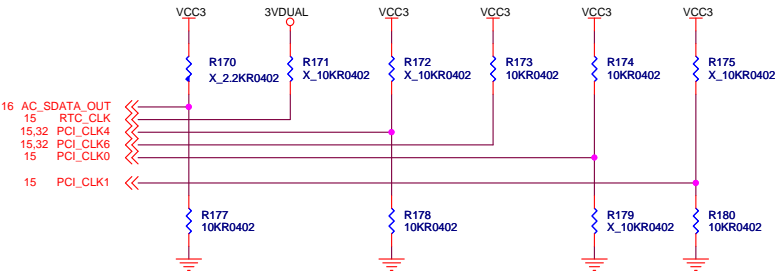
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| SB600-SATA/IDE/HWM/SPI                                                                                         | 0A                                                              |
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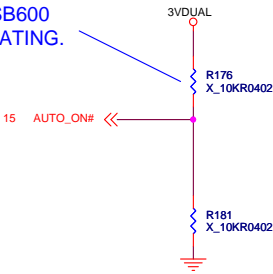


# REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT,  
15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS  
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE  
REQUIRED



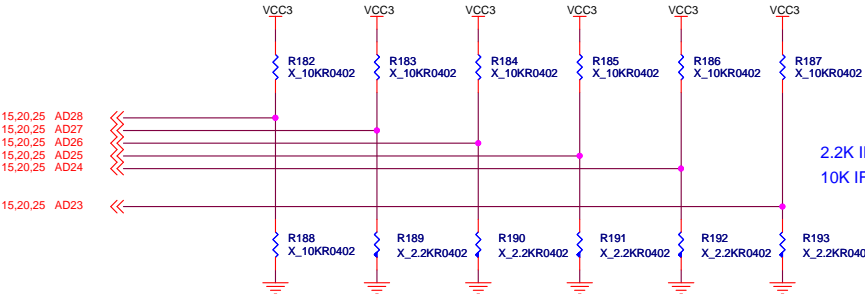
NOTE: R PU RESISTOR FOR  
RTC\_IRQ# IS REQUIRED FOR SB600  
TO KEEP THE INPUT FROM FLOATING.



| SB600     |                                |                         |                           |                      |                                                                                   |          |
|-----------|--------------------------------|-------------------------|---------------------------|----------------------|-----------------------------------------------------------------------------------|----------|
|           | AC_SDOUT                       | RTC_CLK                 | PCI_CLK4                  | PCI_CLK6             | PCI_CLK0                                                                          | PCI_CLK1 |
| PULL HIGH | USE DEBUG STRAPS               | INTERNAL RTC<br>DEFAULT | USE INT. PLL48            | CPU IF=K8<br>DEFAULT | ROM TYPE:<br>H, H = PCI ROM<br>H, L = SPI ROM<br>L, H = LPC ROM<br>L, L = FWH ROM | DEFAULT  |
| PULL LOW  | IGNORE DEBUG STRAPS<br>DEFAULT | EXTERNAL RTC            | USE EXT. 48MHZ<br>DEFAULT | CPU IF=P4            |                                                                                   |          |

# DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



2.2K IF USED FOR SB600.  
10K IF USED FOR SB460.

|           | PCI_AD28                  | PCI_AD27               | PCI_AD26                 | PCI_AD25               | PCI_AD24                           | PCI_AD23                          |
|-----------|---------------------------|------------------------|--------------------------|------------------------|------------------------------------|-----------------------------------|
| PULL HIGH | USE LONG RESET<br>DEFAULT | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | BOOTFAILTIMER DISABLED<br>DEFAULT |
| PULL LOW  | USE SHORT RESET           | BYPASS PCI PLL         | BYPASS ACPI BCLK         | BYPASS IDE PLL         | USE EEPROM PCIE STRAPS             | BOOTFAILTIMER ENABLED             |

SB600 ONLY

SB600 ONLY

FOR SB460,  
PCI\_AD23 IS  
RESERVED

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|----------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------------------------------------------------|
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```

IDSEL = AD18
MASTER = PCI_REQ#0
 PCI_GNT#0

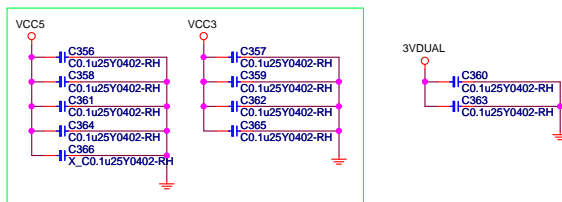
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```

IDSEL = AD19
MASTER = PCI_REQ#1
 PCI_GNT#1

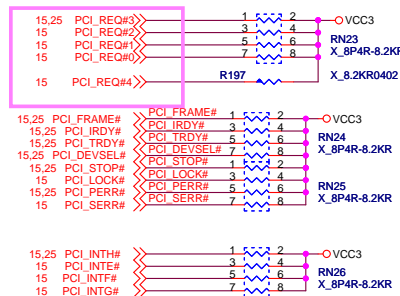
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## PCI SLOT DECOUPLING CAPACITORS

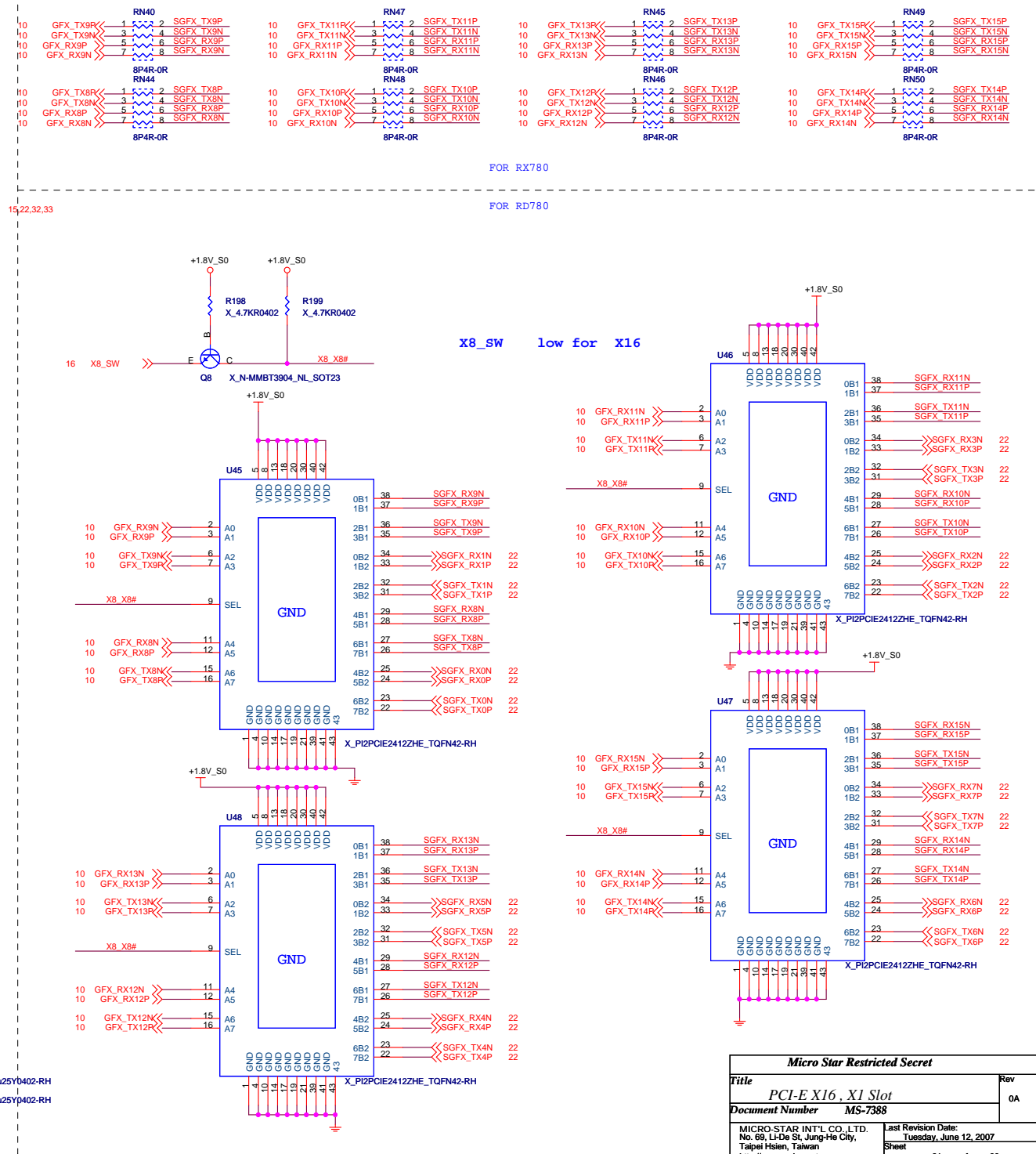
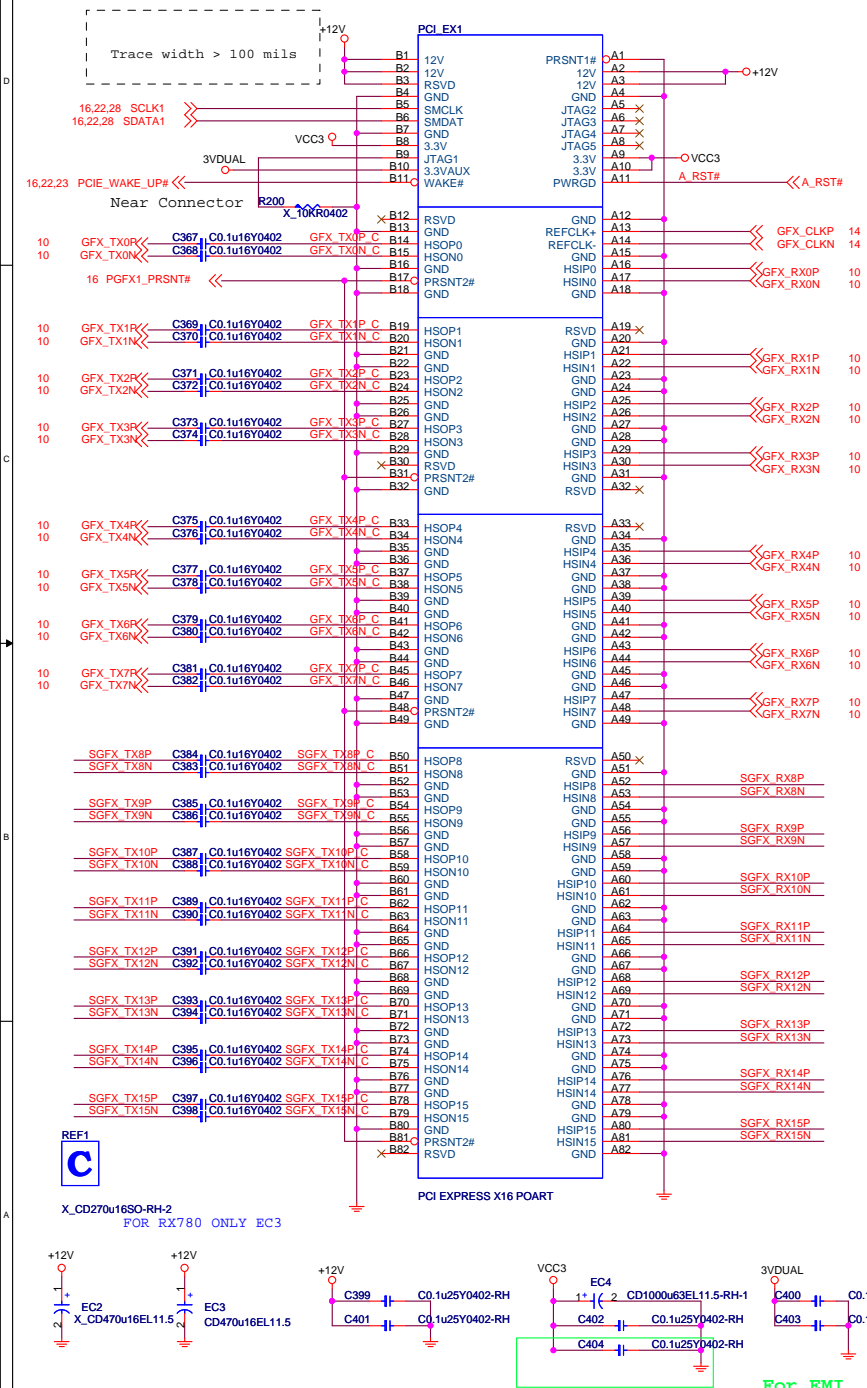


For EMI

## PCI PULL-UP / DOWN RESISTORS

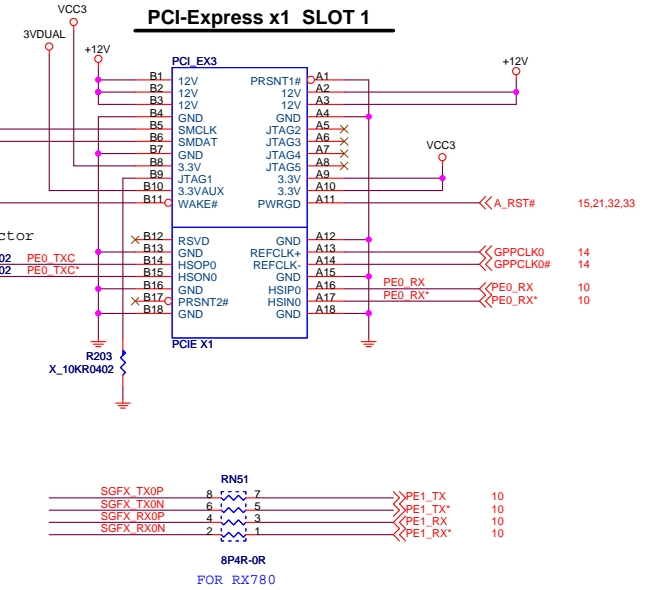
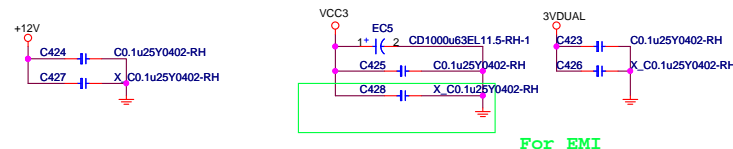
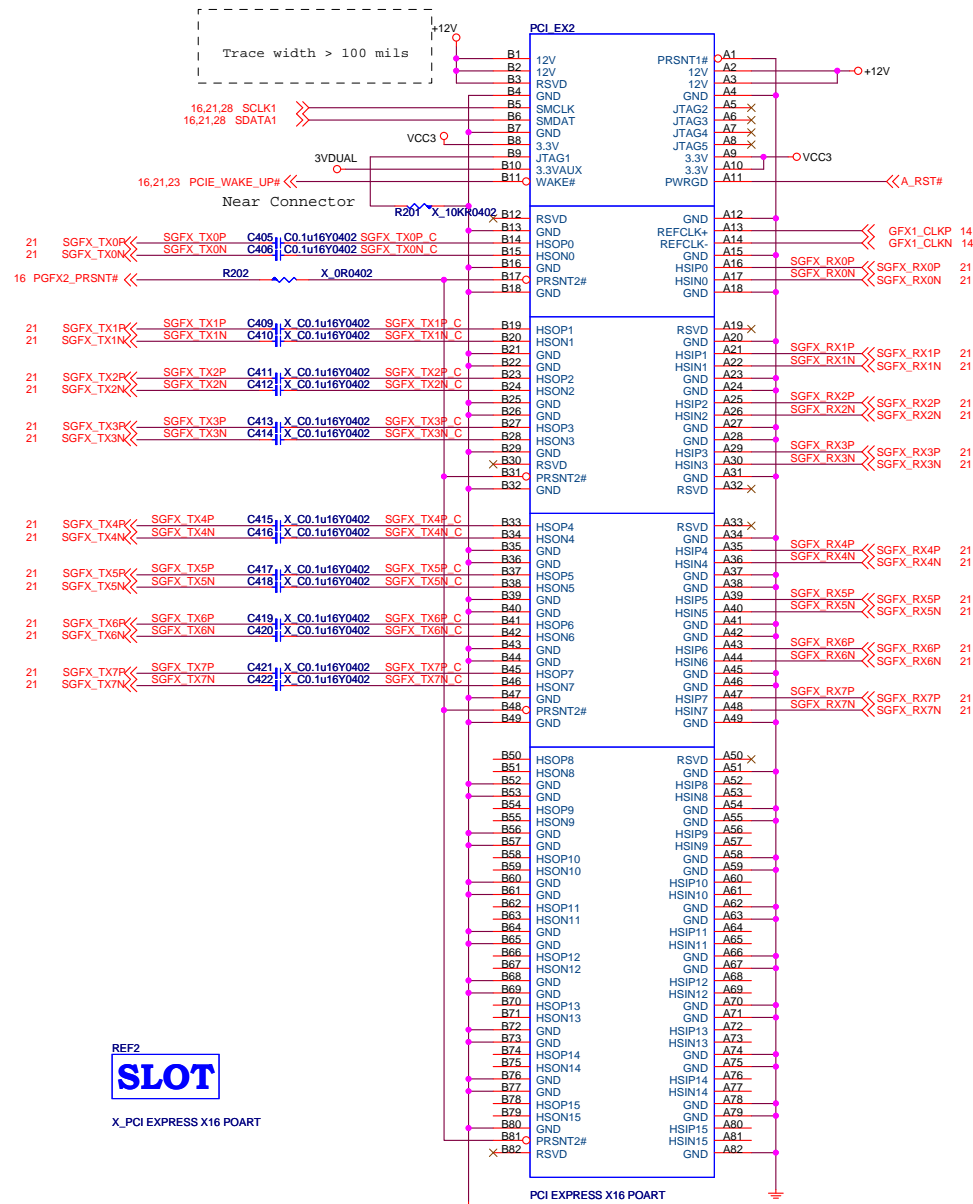


## PCI EXPRESS\_16



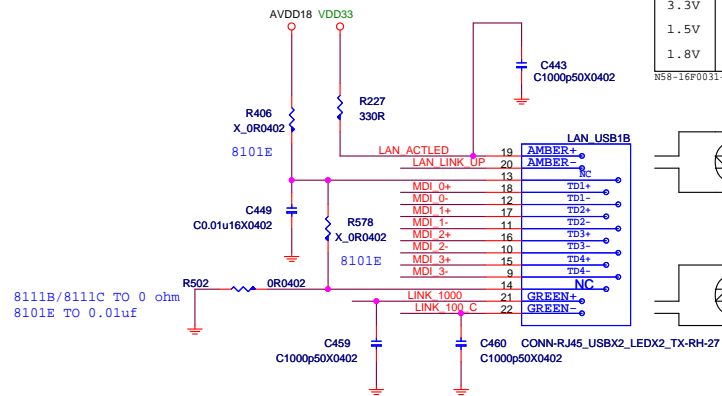
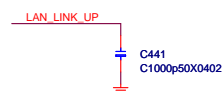
# PCI EXPRESS 16

FOR RX780 PCI-EX1

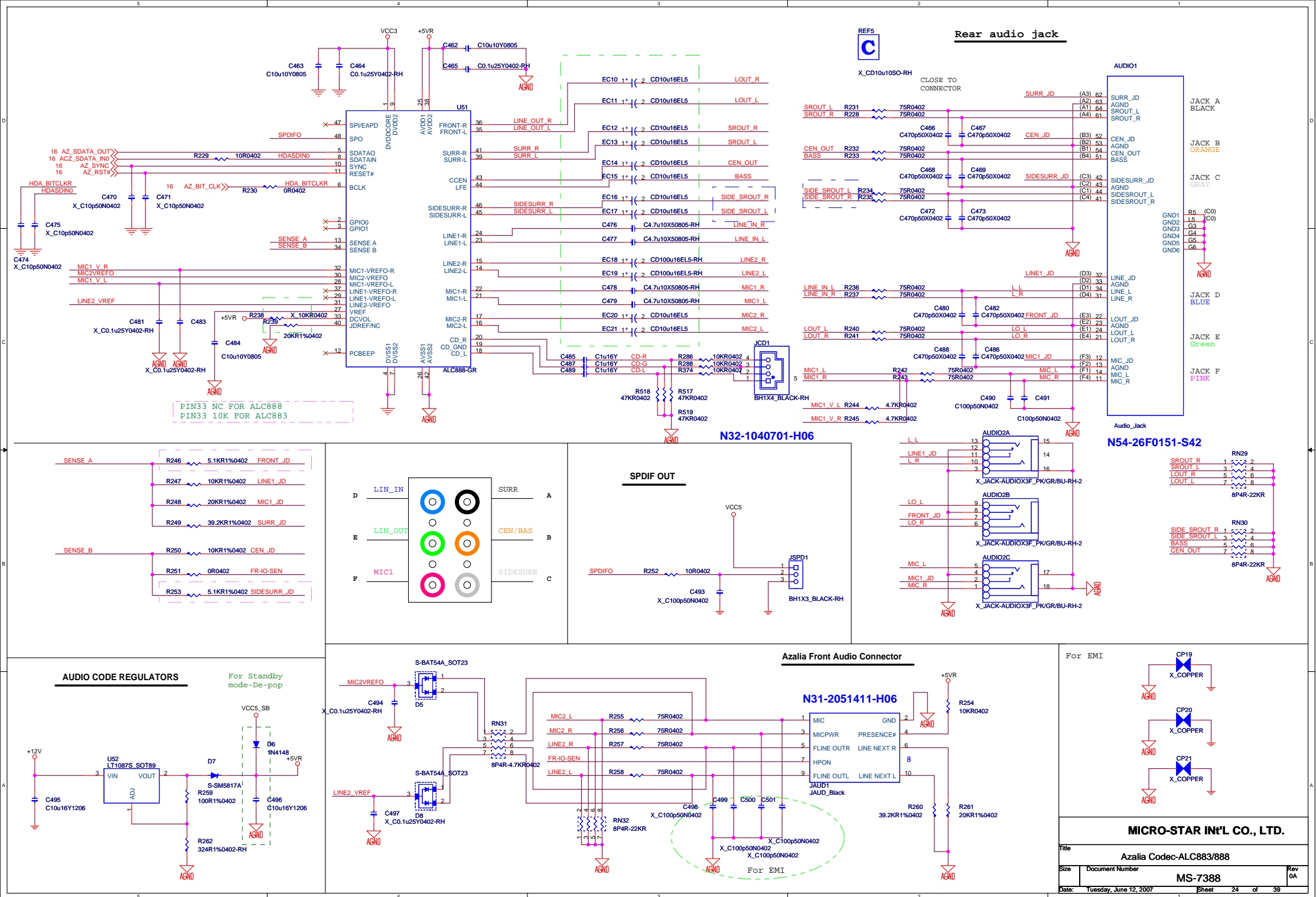


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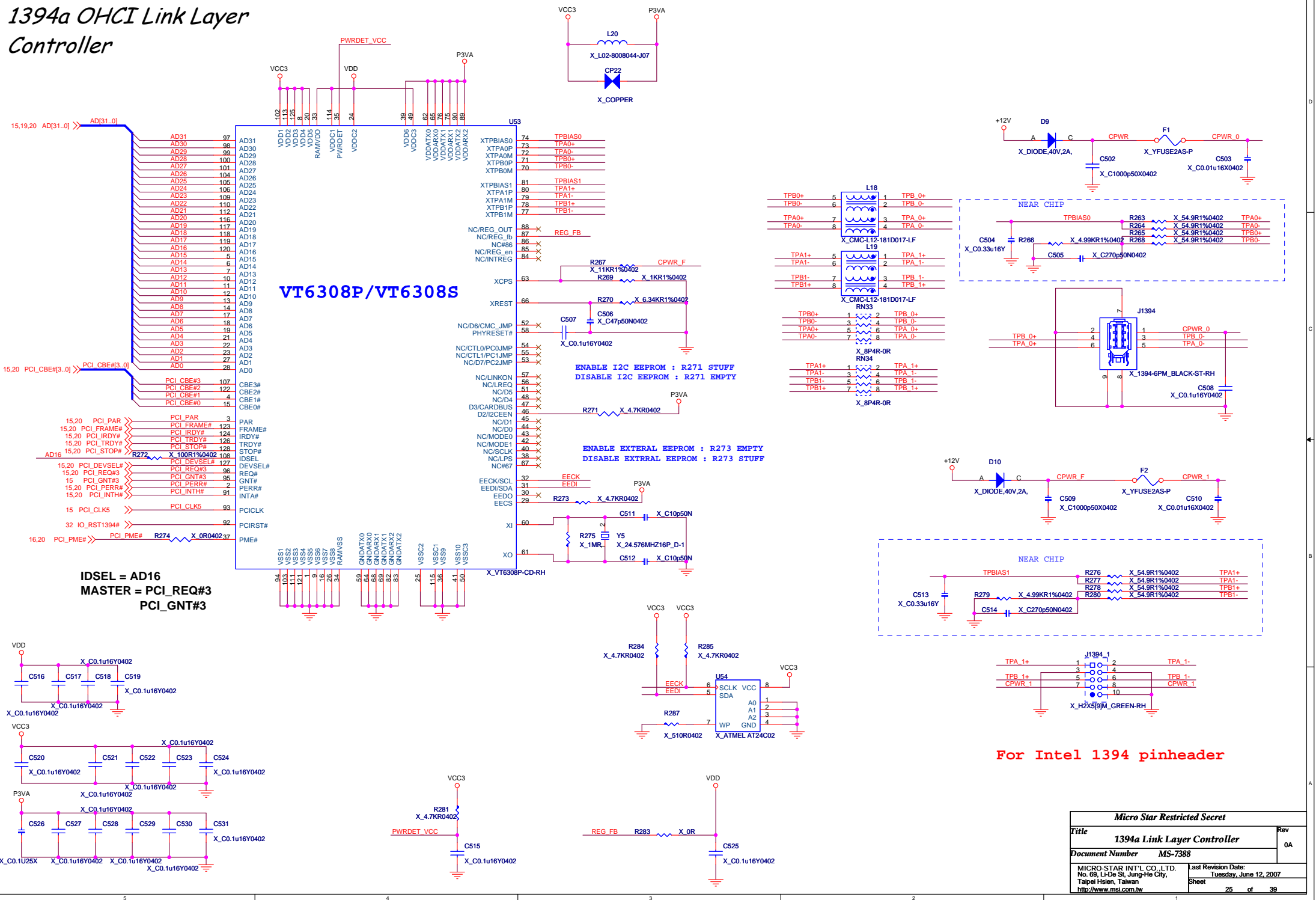




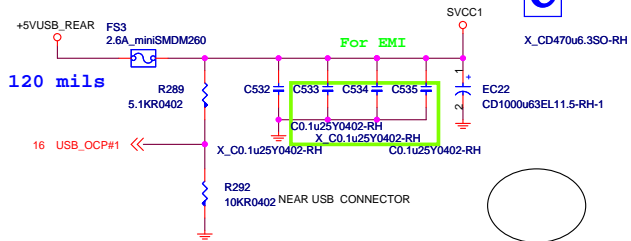
|                                                                                                                                                    |                                                        |
|----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|
| <b>Document Number</b> MS-7388                                                                                                                     |                                                        |
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|                                                                                                                                                    | <b>Sheet</b><br>23 of 39                               |



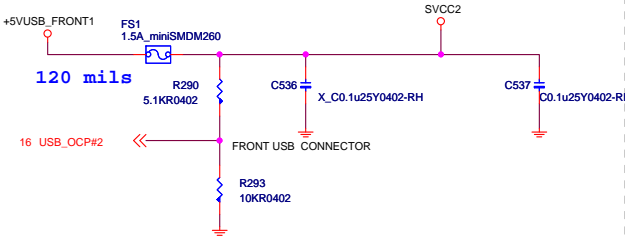
# 1394a OHCI Link Layer Controller



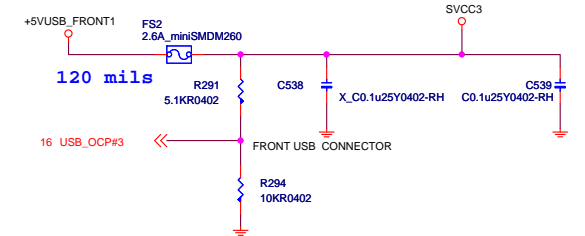
## POWER CIRCUIT FOR USB PORT 0,1



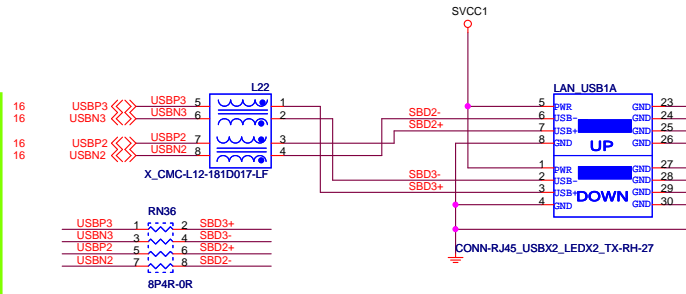
## POWER CIRCUIT FOR USB PORT 4,5



## POWER CIRCUIT FOR USB PORT 6,7,8,9



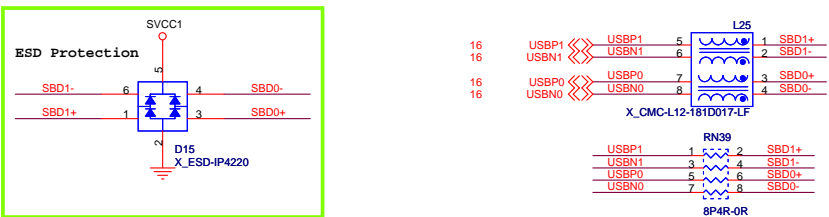
## REAR PANEL USB CONNECTOR FOR USB PORT 2,3



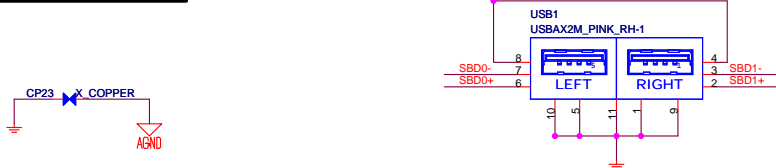
### NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## REAR PANEL USB CONNECTOR FOR USB PORT 0,1



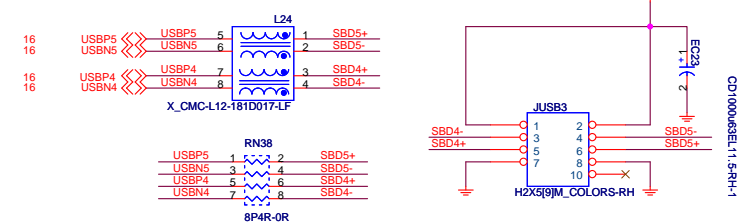
## EMI TEST



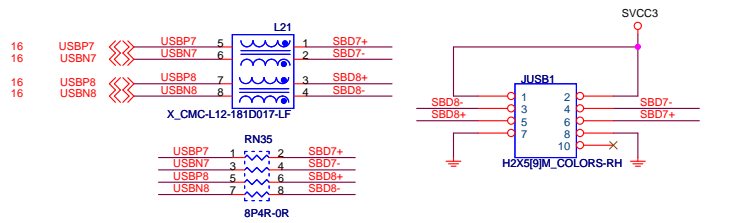
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

## FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

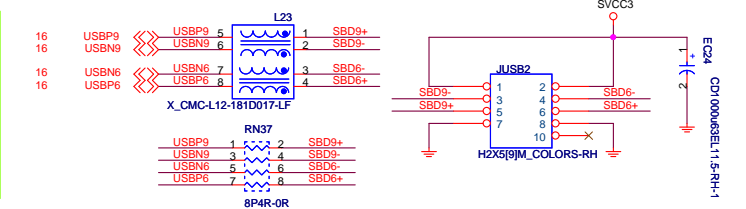
Reversed, can be taken off riser card within bead



## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

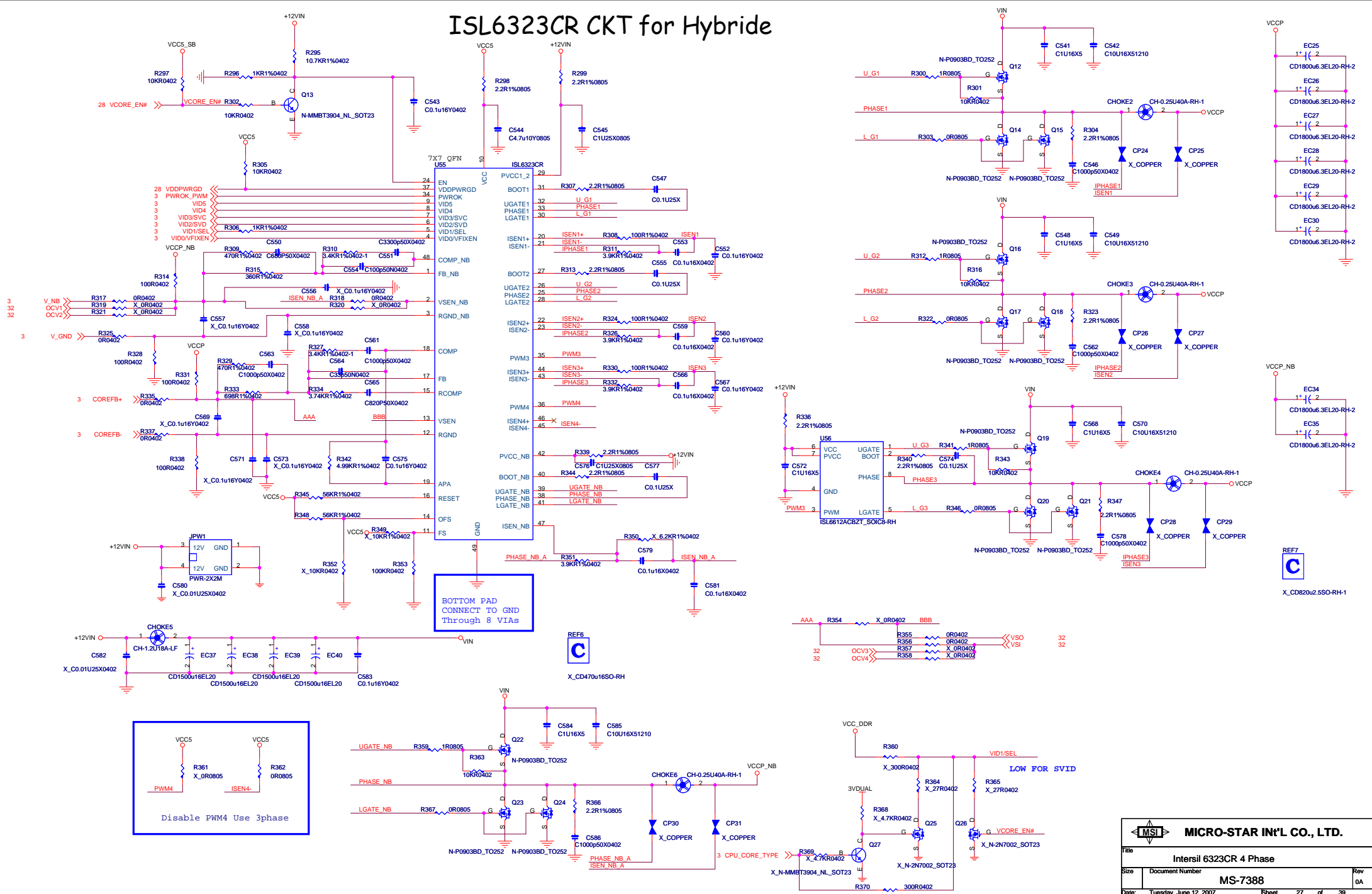


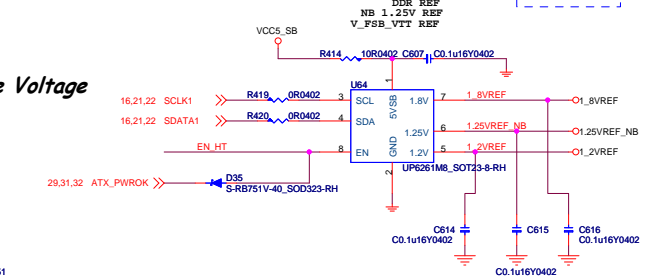
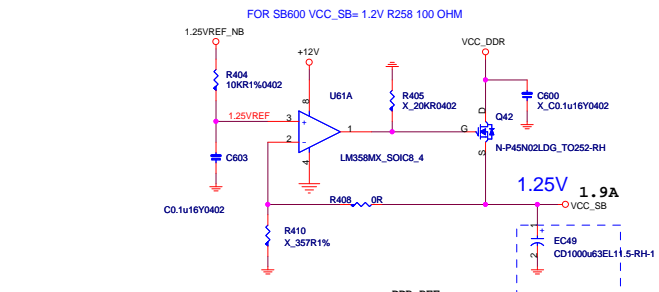
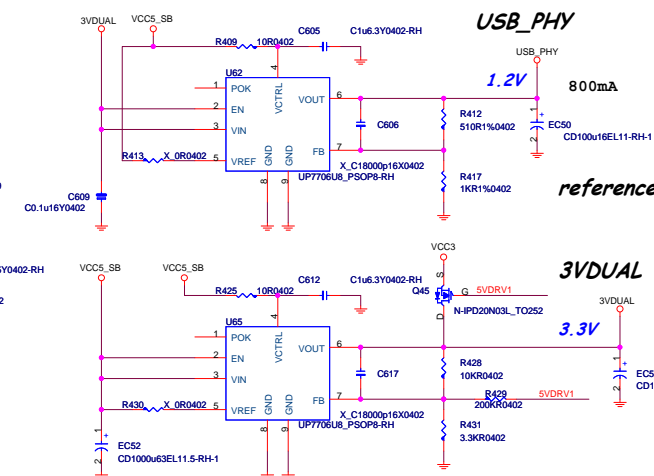
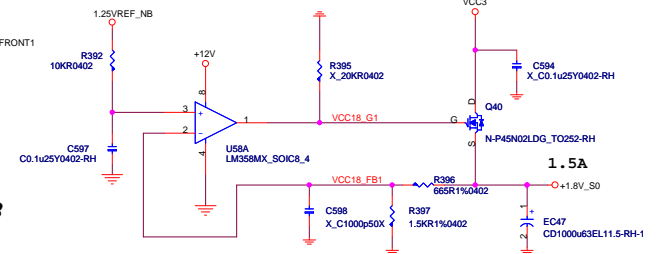
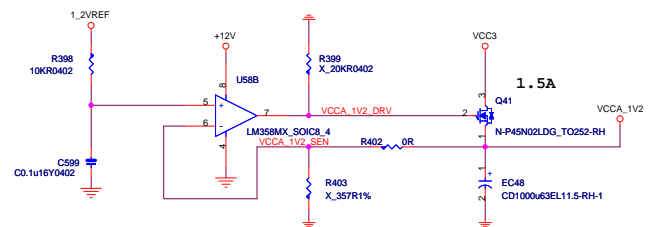
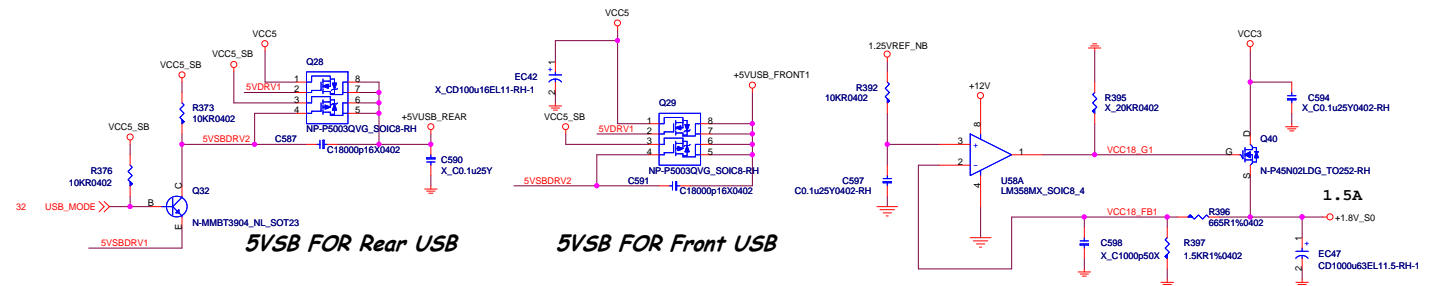
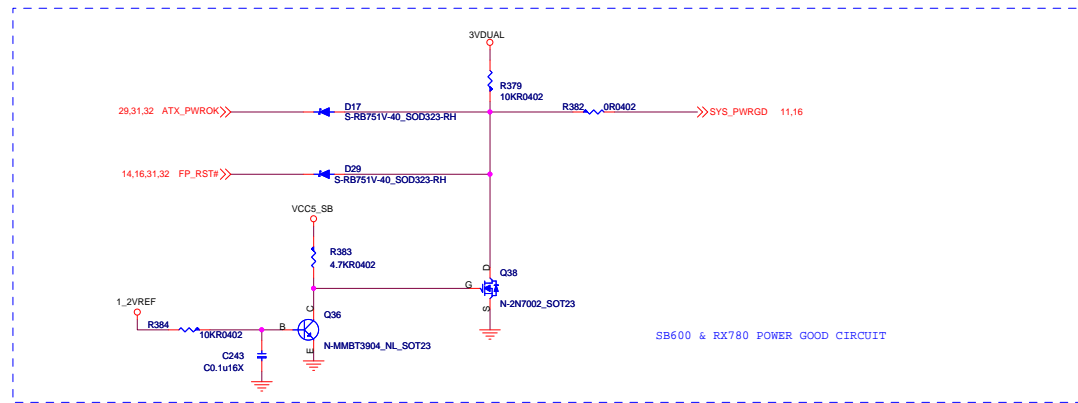
## FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



|       |                        |                                   |          |
|-------|------------------------|-----------------------------------|----------|
| MSI   |                        | <b>MICRO-STAR INT'L CO., LTD.</b> |          |
| Title |                        | USB CONNECTORS                    |          |
| Size  | Document Number        | MS-7388                           |          |
| Date  | Tuesday, June 12, 2007 | Sheet                             | 26 of 39 |

## ISL6323CR CKT for Hybride



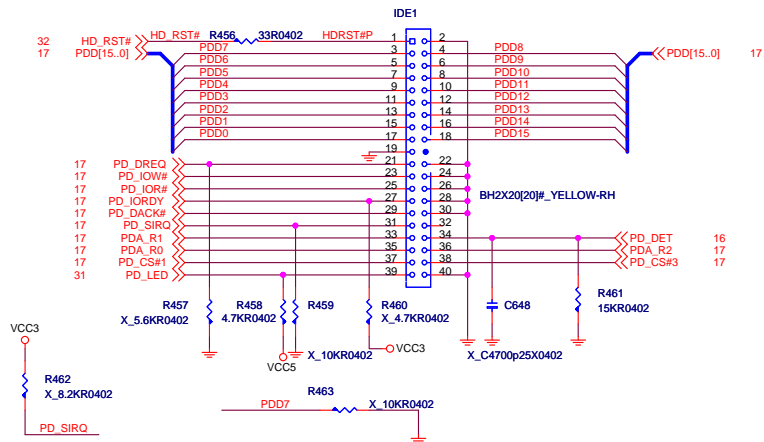


|                                                                                                      |                    |                                                                                            |
|------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------------------------------------------|
| <b><i>Micro Star Restricted Secret</i></b>                                                           |                    |                                                                                            |
| <b>Title</b>                                                                                         | <b>ACPI BY UPI</b> | <b>Rev</b>                                                                                 |
| <b>Document Number</b>                                                                               | <b>MS-7388</b>     | <b>0A</b>                                                                                  |
| MICRO-STAR INT'L CO., LTD.<br>No. 69, Li-De St, Jung-He City,<br>Taipei Hsien, Taiwan<br>Hsinchu 300 |                    | <b>Last Revision Date:</b><br><b>Tuesday, June 12, 2007</b><br><b>Sheet</b> 28    of    30 |

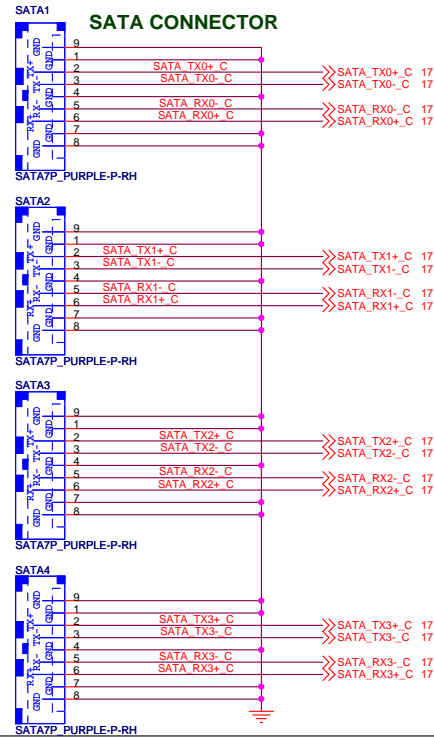




## IDE 1



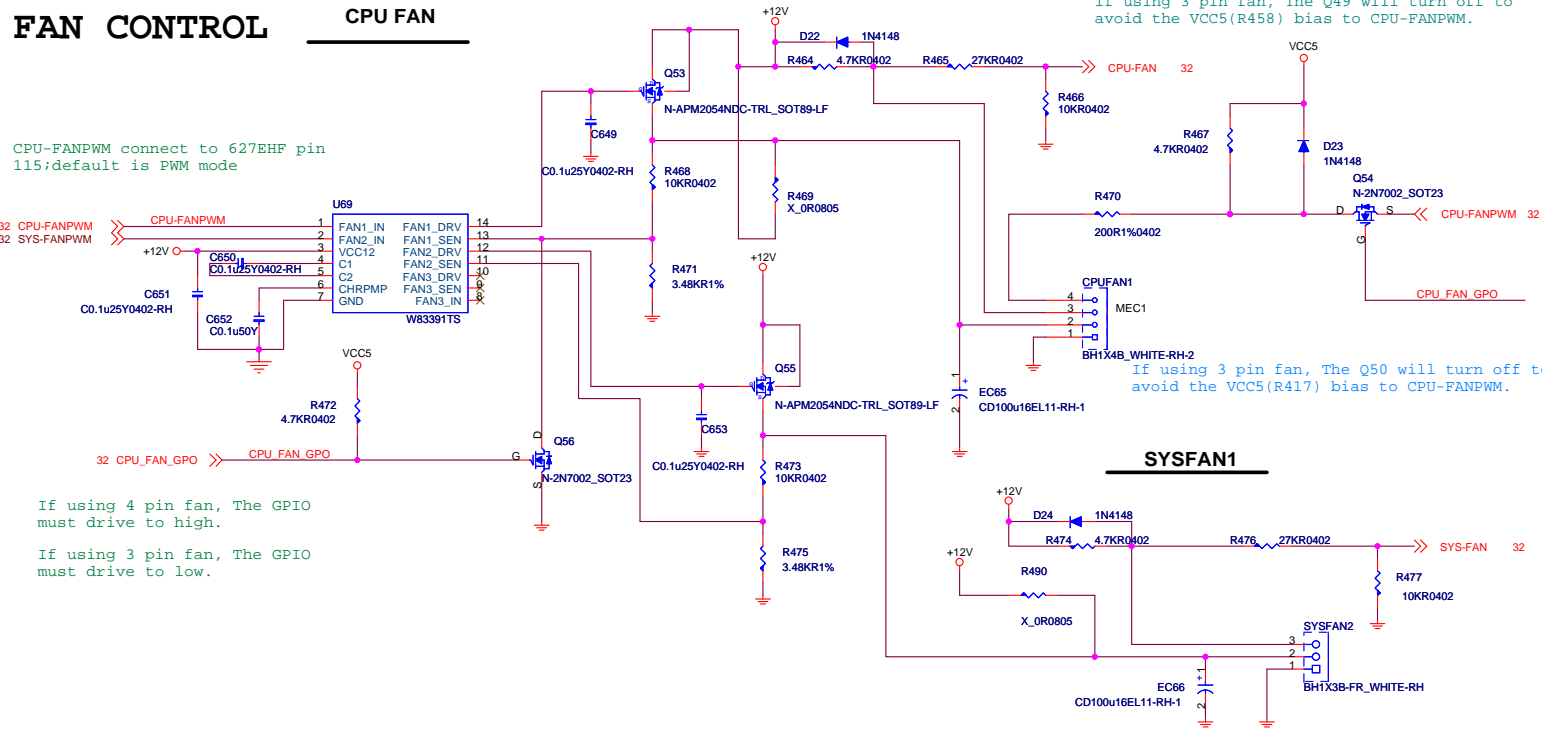
## SATA CONNECTOR



## FAN CONTROL

### CPU FAN

CPU-FANPWM connect to 627EHF pin 115; default is PWM mode



If using 4 pin fan, The GPIO must drive to high.

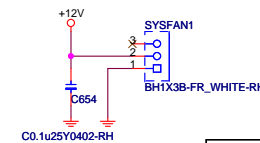
If using 3 pin fan, The GPIO must drive to low.

If using 3 pin fan, The Q49 will turn off to avoid the VCC5(R458) bias to CPU-FANPWM.

If using 3 pin fan, The Q50 will turn off to avoid the VCC5(R417) bias to CPU-FANPWM.

### SYSFAN1

### SYS FAN



| Micro Star Restricted Secret    |  |                        |  |
|---------------------------------|--|------------------------|--|
| Title                           |  | Rev                    |  |
| IDE Conn/FAN/LPT/SATA           |  | 0A                     |  |
| Document Number                 |  | MS-7388                |  |
| MICRO-STAR INT'L CO., LTD.      |  | Last Revision Date:    |  |
| No. 68, Li-Ho St, Jung-Ho City, |  | Tuesday, June 12, 2007 |  |
| Taipei Hsien, Taiwan            |  | Sheet                  |  |
| http://www.msi.com.tw           |  | 30 of 39               |  |

## Intel Front Panel



|                                                                                                                                                                                |                                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| <b><i>Micro Star Restricted Secret</i></b>                                                                                                                                     |                                                                                                |
| <b>Title</b><br><b><i>ATX connector / Front Panel/KB</i></b>                                                                                                                   | <b>Rev</b><br><b>0A</b>                                                                        |
| <b>Document Number</b><br><b><i>MS-7388</i></b>                                                                                                                                |                                                                                                |
| <b>MICRO STAR INT'L CO. LTD.</b><br><b>No. 69, Li-De St., Jung-He City,</b><br><b>Taipei Hsien, Taiwan</b><br><b><a href="http://www.msi.com.tw">http://www.msi.com.tw</a></b> | <b>Last Revision Date:</b><br><b>Tuesday, June 12, 2007</b><br><b>Sheet</b><br><b>31 of 39</b> |



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